

Basic Electrical Engineering II
EE 302L
Experiment 2
Minimization using Karnough Maps and some MSI
Components

1 Objectives

1. Using Karnough maps to find minimal 2-level implementation,
2. investigating both SOP and POS implementations, and
3. Exploring some MSI components

2 Equipment Needed

The student is required to determine the equipment and components which he or she will need to build the circuits and complete the experiments. Since all of the standard chips ever manufactured will not be available to you on the day of the lab, a circuit diagram is sufficient for your pre-lab. Your lab report should include a *schematic* of the circuits that you actually build. A schematic differs from a circuit diagram in that the schematic has **pin numbers**, **part numbers**, and **unit numbers**.

3 Preliminary Procedure

To be completed *before* your lab meets:

1. Design all circuits.
2. Bring with you to lab:
 - A circuit diagram for all circuits which you will actually build using standard integrated circuit components
3. Before starting lab, have your TA initial your circuit diagrams. to show that you came prepared. Lab time is for building and debugging, not for initial design.

4 Procedure

4.1 Design

Consider the function F given by

$$f(a, b, c, d) = \sum m(0, 1, 2, 4, 5, 6, 8, 9, 10)$$

Using a Karnaugh map, determine the minimum sum-of-products implementation for F . Assume that complemented inputs will be available. Draw this circuit as it would be implemented with AND gates and OR gates (and as many inverters as required). Also draw it as it would be implemented using only NAND gates and inverters.

Now determine the minimum product-of-sums implementation of F , again assuming that complemented inputs will be available. Draw this circuit as it would be implemented using OR gates and AND gates (and as many inverters as required). Also draw it as it would be implemented using only NOR gates and inverters.

4.2 Breadboard Procedure

1. Don't forget to have your TA initial your circuit diagrams and schematics to show that you came to lab prepared.
2. Using only NAND gates and inverters, build your sum-of-products circuit from above. Test each input value and record the output in a truth table.
3. Step away from the bench, and allow your *lab partner* to do the rest of the steps in this sub-section.
4. Using only NOR gates and inverters, build your product-of-sums circuit from above. Test each input value and record the output in a truth table.

4.3 MSI Components – Decoders

1. Build a *two-line-to-four-line decoder* as discussed in class. Note that Figure 7.27b of your text shows a larger, *three-line-to-eight-line decoder*.
2. Verify the truth table of the above circuit.
3. The 74x139 chip contains two 2-to-4 decoders with active low outputs and an active low enable for each decoder. A datasheet for this MSI component can be found at:

www.labmaster.com/surplus/parts/html/ic200039-mot/sn741s139d.pdf

Install a 74x139 on your breadboard and verify the truth table of one half of the 74x139.

4. Use an entire 74x139 and whatever other components are necessary to create a 3-to-8 decoder *similar to* that shown in Figure 7.27b of your book. Your 3-to-8 decoder will have active low outputs, so the truth table will be exactly the opposite of that shown in Figure 7.27a of your text.
5. Verify the truth table of your 3-to-8 decoder.

4.4 Complete your First Lab

You should have plenty of time left over this week. Please go back and complete any portions of the first lab that you were unable to complete.

5 Report

1. Include your (original) initialed circuit diagrams in your report so that the TA can readily verify that you have successfully completed the lab exercise.
2. Discuss the results of your minimization. ‘minimal’ (as defined in lecture).
3. Were the outputs of the circuits equal (to those of the other circuits) for all input combinations? Why or why not? Explain.
4. Include your analysis of the final parts of Experiment 1 in this report.