

EE 302L Basic Electrical Engineering II

Experiment 3

Combinational Addition and Subtraction Hardware and Introduction to Sequential Circuits

1 Objectives

1. Verify the functionality of the XOR gate discussed in class.
2. Investigate the “half adder” and “full adder” circuits discussed in class.
3. Experimentally verify that the hardware used for “unsigned binary” addition can be used in 2’s complement addition.
4. Experimentally verify that a simple “adder” circuit can be modified to perform subtraction.
5. Verify the construction of an S-R Latch using only SSI components
6. Learn how to combine *latches* with enables in a Master-Slave configuration to obtain a *flip-flop*

2 Pre-Laboratory Procedure

The student is responsible for reading the lab assignment and determining which portions can be done prior to coming to lab. At there very least you should have circuit diagrams of all circuits you will build.

You should also fill out the four left-hand columns in Table 1 and Table 2 prior to coming to lab. Keep in mind that we are dealing with the *two’s complement* number system in this lab.

2.1 Combinational Adder TTL Procedures

1. Before starting lab, have your TA initial your circuit diagrams and schematics to show that you came prepared. Lab time is for building and debugging, not for initial design.
2. Your TA will provide you with a 74LS86 chip containing 4 exclusive-or gates. Verify the functionality of one of these gates (as discussed on page 362 of your text).

- Using the above chip and some other SSI components, construct a two-bit ripple carry adder, similar to that discussed in class. do this by having one partner construct one full adder and the other partner constructing the other full adder.
- Verify that your two-bit adder functions correctly for all possible input combinations. Tabulate these combinations in your lab report.
- Your TA will provide you with an IC which can be used as an adder. This particular IC is may be capable of functioning as *more than* a simple adder, so you will have to consult the TTL data book in order to ensure that it is configured as an adder.
- Use this adder circuit to determine the values required to complete Table 1

Table 1: Two's compliment addition

A		B		Sum A+B			
decimal	binary	decimal	binary	V	C	binary	decimal
1	0001	1	0001	No	0	0010	2
3		1					
0		-8					
-4		5					
6		2					
-8		7					
-6		-2					

- Using as few additional ICs as possible, modify your circuit to make a 4-bit *subtractor*. You should attempt to design this circuit well before lab so that you can consult the instructor and the TA if you have problems. Some hints will be given in lecture on September 24th.
- Using your subtracter circuit, complete Table 2.

3 Sequential Breadboard Procedure

- Using only SSI components, construct the Gated SR latch shown in Figure 7.44 of your textbook.
- Verify the correct functioning of your circuit, but do not dis-assemble it.
- Modify your circuit to form a Gated D latch, as discussed in class.

Table 2: Two's complement subtraction

A		B		Difference A-B			
decimal	binary	decimal	binary	V	C	binary	decimal
1	0001	1	0001	No	0	0000	0
3		1					
0		-8					
-4		5					
6		2					
-8		7					
-6		-2					

4. Verify the correct functioning of your circuit, but *do not* dis-assemble it.
5. **Step away from the bench, and allow your *lab partner* to do the rest of the steps in this section.** Please make sure that both partners understand, and are capable of reproducing, all steps.
6. The second team member should build *another* D latch by adding a chips as needed. Try to make use of some of the unused components i from the chip(s) already on the board.
7. The two latches should be combined in a “master-slave” fashion to form a positive edge triggered D flip-flop. This circuit should be in your notes, as it was discussed in lecture.
8. Verify the correct operation of this circuit before calling your TA over to demonstrate it to him. He will initial your schematic again to indicate that the circuit was built successfully

4 Report

In addition to your basic lab report, make sure to:

1. Include your (original) initialed circuit diagrams in your report so that the TA can readily verify that you have successfully completed the lab exercise.
2. Determine the *unsigned binary* interpretation of the bit patterns you determined in Table 1 and Table 2. Discuss the use of the two's complement circuit in unsigned binary addition and subtraction.