

EE 245 –Digital Systems Design
Department of Electrical Engineering – Spring 2009

- Instructor:** Dr. Robert Fourney, 215 Harding Hall, 688 – 4016
E-Mail: Robert.Fourney@ieee.org
Home Phone: (given in class) (Call only **before 9 pm and after 9 am on weekends!**)
- Class Web Page:** Web Page: <http://www.engineering.sdstate.edu/~fourneyr/S09/ee245>
- Communication:** We will use several different methods to keep in touch this semester, including announcements in class, email, and the class web page. While I will try to use redundant sources to convey important information, you are responsible for all information regardless of how it is made available.
- Class Meets:** MWF 11:00 – 11:50 AM in Crothers 351
- E-Mail:** My email address is at the top of this page. You are required to check your email and reference the class web page every day (you should “reload” or “refresh” so as to view the most recent version). Your first assignment is to consult the class web page, read the linked essays, and then send me an email stating that you have done this. I will use your email, from your preferred email account, to construct an email list for this class. In the subject line write: “EE245 -- Add to List”.
- Office Hours:** To be determined (with your input) the first week of class. Once established, these hours will be posted to the web page (above) and announced in class. You can also use email or the telephone to either ask questions or to make an appointment to see me if the office hours are not convenient. Please **do not call my home number after 9 pm on any evening or before 9 am on weekends.**
- Text:** *Fundamentals of Digital Logic with Verilog Design.* (2nd edition) by Stephen Brown and Zvonko Vranesic. Published by McGraw Hill.
- Co-requisite:** EE 245L (Digital System Design Laboratory) must be taken concurrently with this class. Either CSc 218 or CSc 150 must be taken either before, or at the same time as this class.
- Objectives:** Students who successfully complete EE 245 will be able to:
1. Convert decimal, binary, and hexadecimal numbering systems from one radix to another; perform basic mathematical operations on binary and hexadecimal numbers; and use Boolean algebra and DeMorgan's theorems to simplify complex logic circuits,
 2. Design digital systems to meet desired needs using standard IC logic gates as well as combinatorial and sequential logic ICs,
 3. Design combinatorial logic circuits such as decoders, encoders, multiplexers, and demultiplexors as well as sequential circuits such as registers, counters, and other finite state machines,
 4. Develop logical expressions given a set of inputs and the required outputs. Students will be able to use Boolean algebra, DeMorgan's theorems, and Karnaugh maps to simplify complex

- logic expressions; and analyze the operation of circuits such as: flip-flop circuits, combinatorial and sequential logic circuits, half- and full-adder circuits, etc,
5. Effectively and professionally communicate using both oral and written methods, and
 6. Write HDL (in our specific case, Verilog HDL) code to describe and implement basic logic gates, MSI components, and finite state machines on a programmable logic device.

Topics: See the course web page for the topics to be covered as well as assigned readings and homework problems.

Grading: Evaluation of student progress will be made, and the final grade determined, using the following scale. Details are given in the following sections.

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| Hour Exam #1 | 20% |
| Hour Exam #2 | 20% |
| Homework (and Quizzes) | 10% |
| Participation (and Quizzes) | 5% |
| Design Lab Practical(s) | 10% |
| Lab/Computer Projects, Demos, and Reports | 20% |
| Comprehensive Final | 15% |

Students are expected to attempt all assignments and exams. ***Failure to complete ALL assignments will adversely affect your grade. Failure to earn at least a “C” in the lab (245L) will result in you failing this class.***

Final letter grades for the course will be determined by plotting the cumulative points earned by each individual student and normalizing the letter grades relevant to the other students and to my expectations. If it makes sense to do so, I will try to place the cut-offs between letter grades in the gaps so that two students having approximately the same overall score will not be assigned different letter grades. Note that it is **not always possible** to do this.

Homework: Homework assignments will be given. Not all problems will be graded, but you will not know in advance which problems will be graded. I may give a quiz on the previous week’s homework in lieu of **or in addition to** grading the homework. These quizzes will count towards the “Homework” portion of your grade. While homework is normally due at the beginning of class on a specified day, you can **expect a quiz at any time.**

Homework Format: All homework problems must be neatly and legibly completed on non-spiral paper. I reserve the right to impose further restrictions and specifications if I am not happy with the quality of homework submissions. Note that **failure to follow the specified format may result in a grade reduction.**

Participation: A student’s success in this course will depend greatly upon his/her attendance and participation. In the event that a student must miss class, advance notice to the instructor is expected. Class notes should be obtained from those in attendance. Attendance will be reflected in the “class participation” portion of your final grade. We will sometimes have a short quiz on the basic concepts as we are discussing them.

Such quizzes, on relatively new material, will be included in your “class participation” grade. In summary, detailed quizzes on previous homework will count towards “homework” and broad quizzes on current topics will count towards “participation”. However, since both types of quizzes may be unannounced, unexcused absences can also adversely effect your homework grade! For these, and many other, reasons **it is in your best interest to attend all scheduled class sessions.**

Design Lab Practical: At some point during the second half of the semester, you will be asked to design and implement a small circuit. This will be done in real time, probably with me looking over your shoulder. This will give you a chance to show me that you have a basic grasp of the design methods we are studying, and that you (and not just your lab partner) know how to use the equipment and software in the lab. You will work alone on this, and it will be graded on an “all-or-nothing” basis with very little partial credit. I will attempt to design and schedule the assignment so that time should not be a factor, and allow (much) more time than I think will be required. You will be allowed to demonstrate the circuit at any time, and if it is not correct you will be allowed to continue working on it up to the time limit.

Lab Projects and Reports: You will also have several design projects, each of which may consist of several parts with separate deliverables and due dates. Due to the learning curve in the class, most of this effort will be during the second half of the semester *but* it is important to get started on each project as early as possible. To help you get started at the appropriate time, a portion of the project grade may be assigned to either a proposal or preliminary design document which you will present to me. This may involve a written document and/or an oral presentation to (some of) your classmates.

Exams: Exam format will be closed textbook & notes. I may provide you with some relevant reference material during the exam, either as part of the problem or as a separate handout. Depending on the exam you probably will not be allowed to use a calculator. The exact format and what is allowed will be made clear prior to the exam. Makeup exams and/or quizzes will be offered only under extreme circumstances **and** with prior permission.

Final exam The Final exam will be given on Monday, May 4th at 9:00 am. This time slot is determined by the SDSU Registrar and is not subject to change.

Special Needs: If you have a documented disability and wish to discuss academic accommodation, you must contact the instructor within the first full week of the class. To learn more about SDSU Disability Services please consult the following web address <http://www3.sdstate.edu/StudentLife/DisabilityServices/>

Honor Code: Each student is expected to maintain a professional attitude and perform to the best of their abilities without resorting to plagiarism, cheating, etc. Violations of academic honor code **will** result in a failing grade for the class. Depending on the severity of the violation, additional penalties may apply.

Freedom in learning: Students are responsible for learning the content of any course of study in which they are enrolled. Under Board of Regents and University policy, student academic performance shall be evaluated solely on an academic basis and students should be free to take reasoned exception to the data or views offered in any course of study. Students who believe that an academic evaluation is unrelated to academic standards but is related instead to judgment of their personal opinion or conduct should first contact the instructor of the course. If the student remains unsatisfied, the student may contact the department head and/or dean of the college which offers the class to initiate a review of the evaluation.