

EE 245: Digital System Design Project 1 Description

1 Overview

Your assignment is to design, describe, and build a vending machine similar to that of the in-class example discussed previously. Your machine should accept nickels, dimes, and quarters. It should dispense a product once 35 cents has been received. Unlike my example in class, your machine *must give change* and *must* be a **Moore-type machine**. You may make reasonable assumptions, but will be penalized for unreasonable assumptions. For example, you may assume that a person with correct change will use the correct change and not put extra money in unless he would benefit from this. You would not therefore have to give change for \$1.00 since the person should have stopped putting in money well before getting to that state. You are *not* to give extra product or change if somebody violates these assumptions, but you may short-change them.

You may work with a single partner (teams of no more than two). Choose your partner wisely. You would be better off working alone than with a person who has yet to show up on lab-day with a schematic and/or a design. This person is probably not going to morph into the ideal project partner overnight. I would prefer for students to work in groups of two (due to limited lab resources and the learning experience of working on a team). If you cannot find a partner, you will be allowed to work alone.

2 Deliverables and Deadlines

Item	Due Date
Preliminary Design Document	4:00 pm Monday March 2
Circuit or Verilog Completed, Tested, and Submitted	8:00 am Monday March 23
Project Demonstration	Be ready by March 24
Final Design Report	Before Class on March 27

2.1 Preliminary Design Report (PDR)

Each team will hand in a preliminary design document by Monday, March 2. This document will include an overview of the approach that you plan to take in solving this problem. This report will include any required state diagrams, transition tables and/or flowcharts. Note that exactly what is required will depend upon your design approach. You do not need to include excitation information, but you should have read and understood the information on five-variable Karnaugh

maps (Section 4.1 of your text). Five- and six-variable Karnaugh maps will be discussed in class very briefly on Friday, February 27th. You might also want to look at the *Quine-McCluskey method* of minimizing logic functions discussed in Section 4.9 of your text. This material will also be discussed in class on Friday, but this project is simple enough that Karnaugh maps should suffice. You should be aware of any constraints imposed by your selected minimization approach and outline the steps that you have taken to ensure that your design will be successful.

You should discuss any assumptions that you are making, and attempt to justify them. For example, if you want to assume that two coins will not be present (on the inputs) at the same time, you need to justify that assumption in your PDR (as well as in your final design report).

You should also include a *schedule* indicating when you plan to meet with your team, when and when you plan to meet significant milestones. (Hint: there are more than just the milestones listed in the table above. There are also some additional confounding aspects of using a pushbutton as a clock. These aspects will be discussed in class next week, and you will be expected to incorporate a solution into your project. Also note that spring break falls between now and when your project is due. Getting started early would be a good idea.)

2.2 Project Demonstration

You will may implement your project using *only structural Verilog* on the Altera DE-2 FPGA proto-boards or using TTL logic. I would advise using the Verilog/FPGA approach for this project. You may use a push-button to simulate a clock signal and three switches to simulate your inputs (nickel, dime, quarter). Use an LED to indicate when a product is to be dispensed, and other LEDs to indicate when each type of change should be returned. You should take a modular approach to your design.

You are to have your project working and tested *before* 8:00 am on Monday, March 23rd. Your tested and fully functional Verilog code should be emailed to EE245Ldsu@gmail.com prior to that time. If you choose to implement the project using TTL your project must be placed into escrow with Dr. Fourney prior to 8:00 am. Note that **you will have another lab assignment to perform during your lab sessions on March 24th**. However, I may ask you to take a short break from that assignment and demonstrate the project at any time during your lab section on Tuesday. Notice that I said “tested”. You will label your switches and LEDs and I will test that your project works. It should obviously work for multiple purchases (not just the first time). It *must not* require a “reset” or extra clock pulse between purchases. It should work for all reasonable inputs (e.g. all reasonable assumptions made and stated in your preliminary design report and final documentation).

2.3 Final Report

Each team will hand in a written final report, no later than class time on Friday, March 27th. This report should include everything I might want to know about your project and the steps you took in designing and building it. Include all of the stuff from the design document, and more. State tables, state diagrams, excitation logic, flow charts, circuit drawings – whatever you needed to complete your design using your chosen approach. Include lessons learned (both EE 245 and life variety). Include a section on how you could improve your project if you had another week to work on it. This is your chance to sell me on your project, so mention any extra features, or anything you feel is extraordinary about your project.