

EE 245: Digital System Design

Project 2 Description

1 Overview

Your assignment is to design, describe, and build a simple processor similar to that discussed in Section 7.14.2 and shown in Figure 7.73 of your textbook. A similar processor is also discussed at:

ftp://ftp.altera.com/up/pub/Laboratory_Exercises/DE2/Digital_Logic/Verilog/lab9_Verilog.pdf

Both the textbook and the above link contain many hints and Verilog samples beyond those discussed in class.

Your processor bus should be 16 bits wide, and you should have 8 general purpose registers, numbered R0-R7, in addition to the “A” and “G” registers.

This implies that you will need three bits to specify each of Rx and Ry. Your function register should also be 16 bits wide, and 16 red LEDs (LEDR15-LEDR0) should be connected to the processor bus. Sixteen switches (SW15-SW0) will be connected to the “Data” wires in Figure 7.73. These will be used to load the various registers, including the “function register” (which I will also refer to as the “instruction register”).

You will implement, and your processor will support, the following functions and the corresponding instruction word formats.

000_0000_XXX_UUU_UUU	Load XXX from the slide switches (Data input) (UUU_UUU is unused): $Rx \leftarrow \text{Data}$
000_0001_XXX_YYY_UUU	Move contents of Register XXX into Register YYY (UUU is unused): $Ry \leftarrow [Rx]$
100_0010_XXX_YYY_UUU	ADD contents of Registers XXX and YYY, placing the result back into Register XXX: $Rx \leftarrow [Rx] + [Ry]$
100_0011_XXX_YYY_UUU	Subtract the contents of YYY from the contents of XXX and store the result into XXX: $Rx \leftarrow [Rx] - [Ry]$
100_0100_XXX_YYY_UUU	Logically OR the bit pattern in Register XXX with that in Register YYY, keeping the result in Register XXX: $Rx \leftarrow [Rx] \mid [Ry]$
100_0101_XXX_YYY_UUU	Logically AND the bit pattern in Register XXX with that in Register YYY, keeping the result in Register XXX: $Rx \leftarrow [Rx] \& [Ry]$
100_0110_XXX_YYY_UUU	Take the bitwise complement of the contents of Register Y and store the result in Register X (Note that XXX and YYY could specify the same register). $Rx \leftarrow \text{ones' comp } [Ry]$
100_0111_XXX_YYY_UUU	Take the two's complement of the contents of Register Y and store the result in Register X (Note that XXX and YYY can specify the same register): $Rx \leftarrow \text{ones' comp } [Ry] + 1$

Additionally, the hex value of the contents of the bus should be displayed on the seven segment display. You should use another push button switch in conjunction with slide switches SW2-SW0 to momentarily display the contents of any of the eight general purpose registers on the seven-segment display. When the button is pressed, the switches select which register to display. When the switch is released the contents of the bus are displayed (remember that the push button switches are active-low). You should also take steps to ensure that your push-button clock is debounced. Recall that most of this functionality was developed as part of a previous lab

You may work with a single partner (teams of no more than two). Choose your partner wisely. I would prefer for students to work in groups of two (due to limited lab resources and the learning experience of working on a team). If you cannot find a partner, you will be allowed to work alone.

2 Deliverables and Deadlines

Item	Due Date
Verilog Completed, Tested, and Submitted	8:00 am Wednesday, April 28
Project Demonstration	You must schedule and demo by COB on April 30
Final Design Report	Before Class on May 1

2.1 Project Demonstration

You shall implement your project using Verilog on the Altera DE-2 FPGA proto-boards. In addition to the switches specified above, you should use switch SW17 as a “run” switch and a push button as a clock. Your clock must be fully debounced, using methods we discussed in class.

You are to have your project working and tested *before* 8:00 am on Wednesday, April 29th. Your tested and fully functional Verilog code should be emailed to *EE245Ldsu@gmail.com* prior to that time. *You* will need to schedule a time to demonstrate your project to me, and all demos must be completed by the end of the school day on Thursday, April 30th. There are other students scheduled in the lab on Thursday, so you will not be able to work on your projects at that time. I will have one workstation set aside for EE 245 demos. As with your pop machine, your processor should not require a “reset” or extra clock pulse between instructions.

2.2 Final Report

Each team will hand in a written final report, no later than class time on Friday, May 1st. This report should include everything I might want to know about your project and the steps you took in designing and building it. Include all information pertaining to the design, and more. State tables, state diagrams, excitation logic, flow charts, circuit drawings – whatever you needed to complete

your design using your chosen approach. Include lessons learned (both EE 245 and life variety). Include a section on how you could improve your project if you had another week to work on it. This is your chance to sell me on your project, so mention any extra features, or anything you feel is extraordinary about your project. Make sure that you **justify any and all assumptions that you made**. Also make sure that you use this opportunity to **cite any and all sources** that you used, including the text book and the web links I've provided.