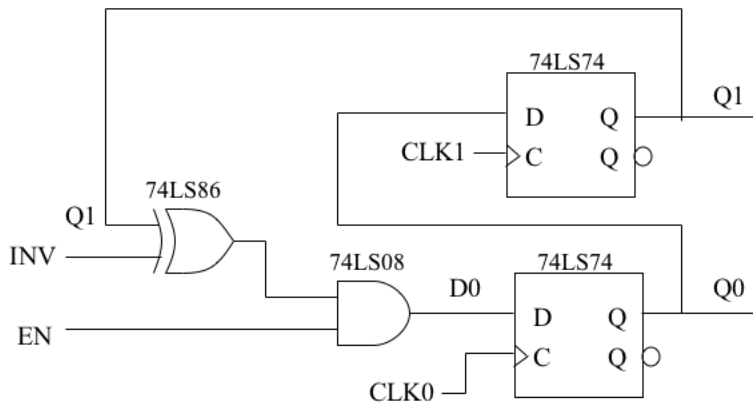


Practice Exam

This was the second exam for a previous semester. In addition to all of the material that was covered for the first exam, you might be expected to answer questions on Verilog, and questions regarding MSI and SSI components.

From last semester's exam, with lots of white space omitted:

Problem 1 : (30 points total)



A) This figure contains a typical sequential circuit. Using the attached timing information, determine the delay from the time that “Q1” transitions from logic “0” to logic “1” until the corresponding change shows up at the output of the and gate (labeled “D0”) Assume that both INV and EN remain at logic value 1 throughout this time, and show all work.

B) Repeat Part A for Q1 going from 1 to 0. Show all work.

C) This circuit is part of a system which is to be clocked with a clock period of 200 nS. Is this clock period long enough (e.g is the clock rate low enough)? If so, specify the setup-time margin. If not, specify the minimum clock period that can be used.

Problem 2: Finite State Machine Design (30 points total)

For this problem, you are to begin the design of a FSM which will detect the pattern 1011 on the single input, X. The output, Z, should be 1 *only* when the input, X, has matched this pattern for the *previous* four clock cycles, *even if the pattern overlaps* another instance of this pattern.

Part A Draw the state diagram for a Moore-type machine that satisfies the above specification. Recall that the outputs of a Moore-type machine depend *only* on the current state.

Part B Assign state variables and show the transition/output table (a transition table that also indicates the output associated with each state. There is an example of this type of table in Problem 3). You should have a row for every combination of state variables, but you may use a minimal cost assignment when dealing with any unused states.

Problem 3: More FSM Design (2 pages, 40 points total)

Consider the transition/output table shown below:

		X		Z
		0	1	
Q1	Q0	01	11	1
	00	11	10	0
	10	00	01	0
	11	10	00	0
		Q1*Q0*		

Part A Design the clocked synchronous state machine with the transition/output table shown above. Use a D flip-flop to implement Q0 and a J-K flip-flop to implement Q1. Show all work, and **draw the the circuit**. You may use any type of gates you desire in addition to the flip-flops. Complete your design, and show your complete circuit, on the next page.

Part B Use the final page of the exam to show how you would implement excitation and output logic of your machine using a PAL16L8. Implement the **active low** versions of D0, J1, K1, Z. You must use the pins that I have labeled for both input and output. You may need to specify connections to assure that my IO selections work properly.

(I attached a copy of the PAL16L8 handout from class for Part B)