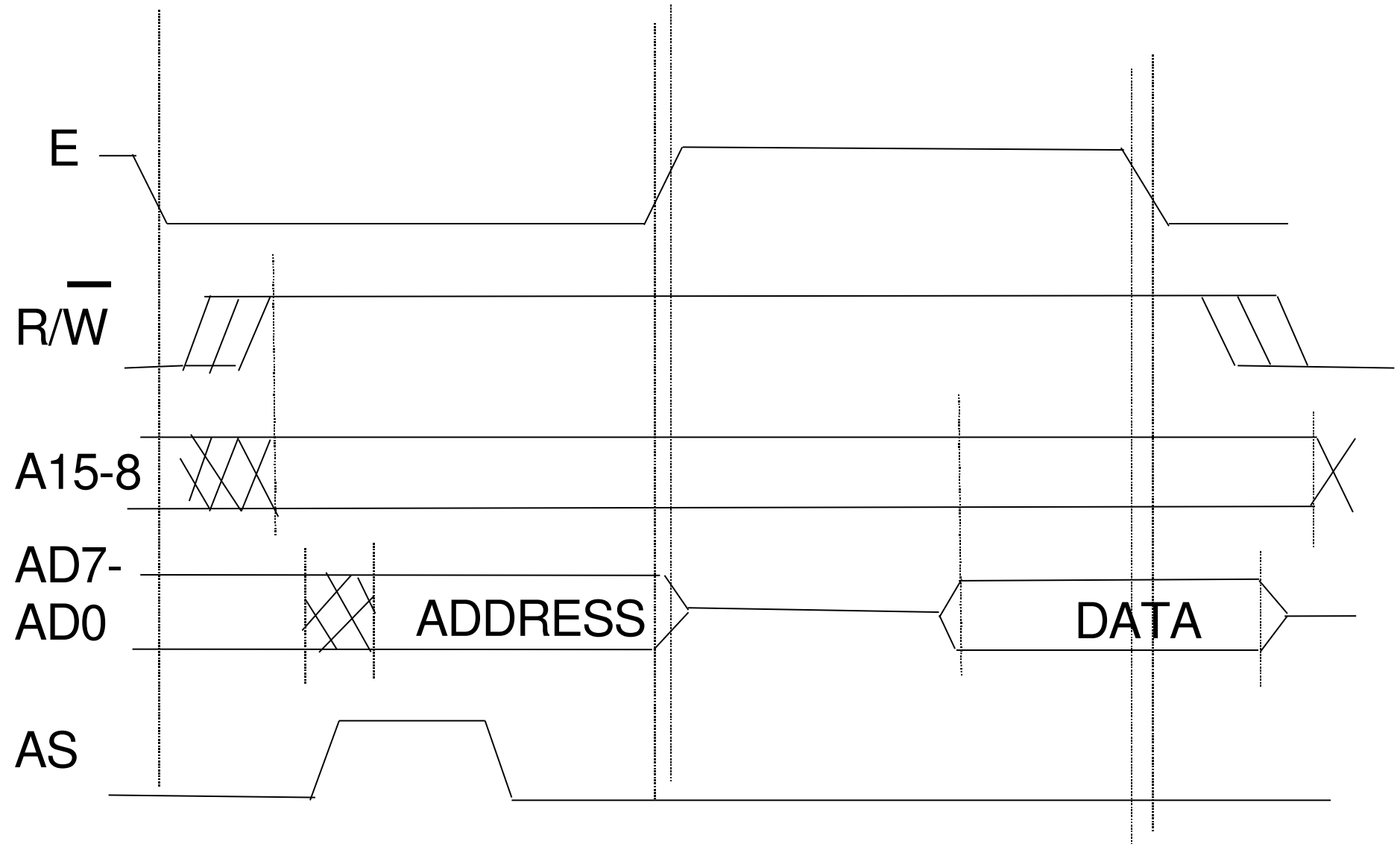
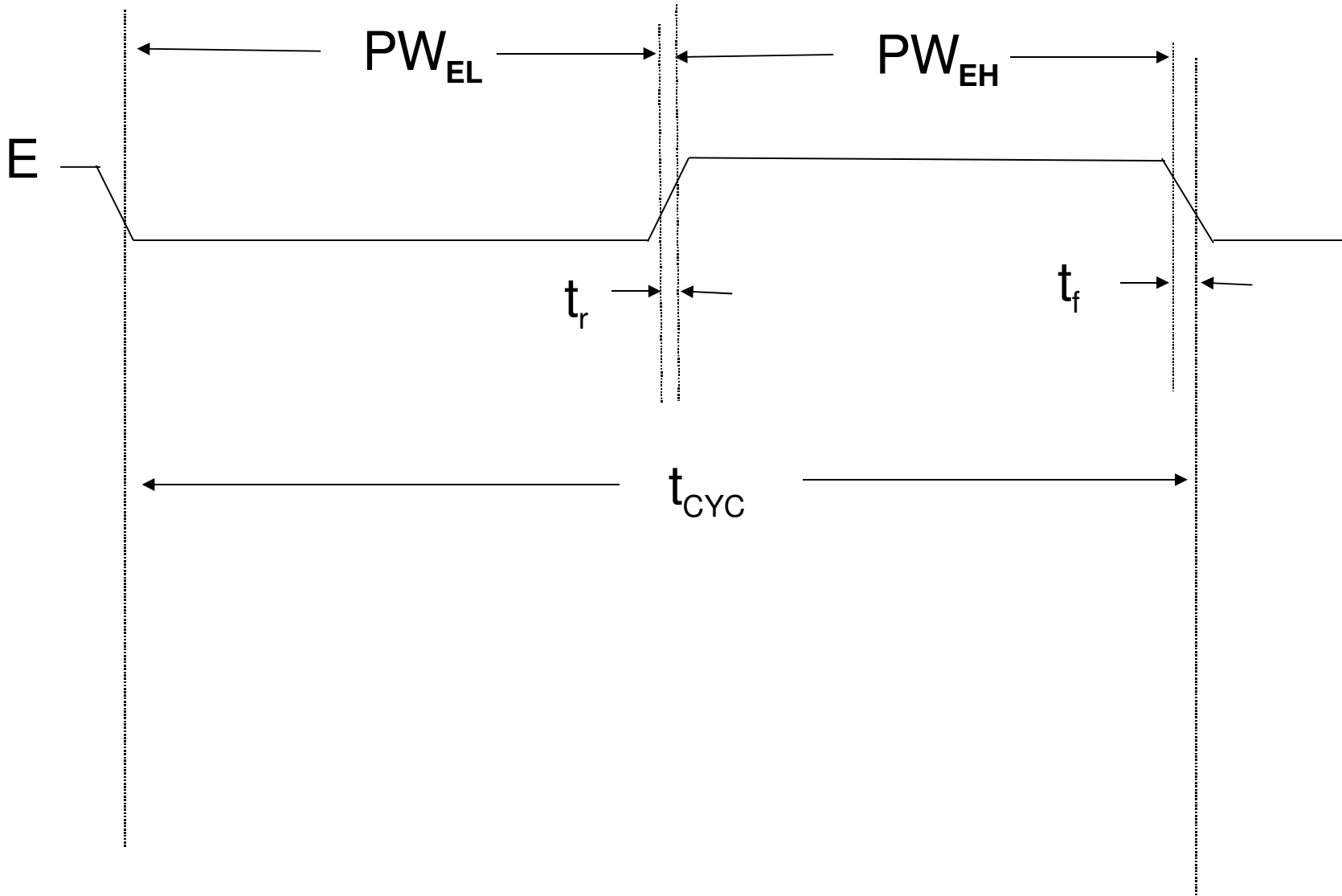


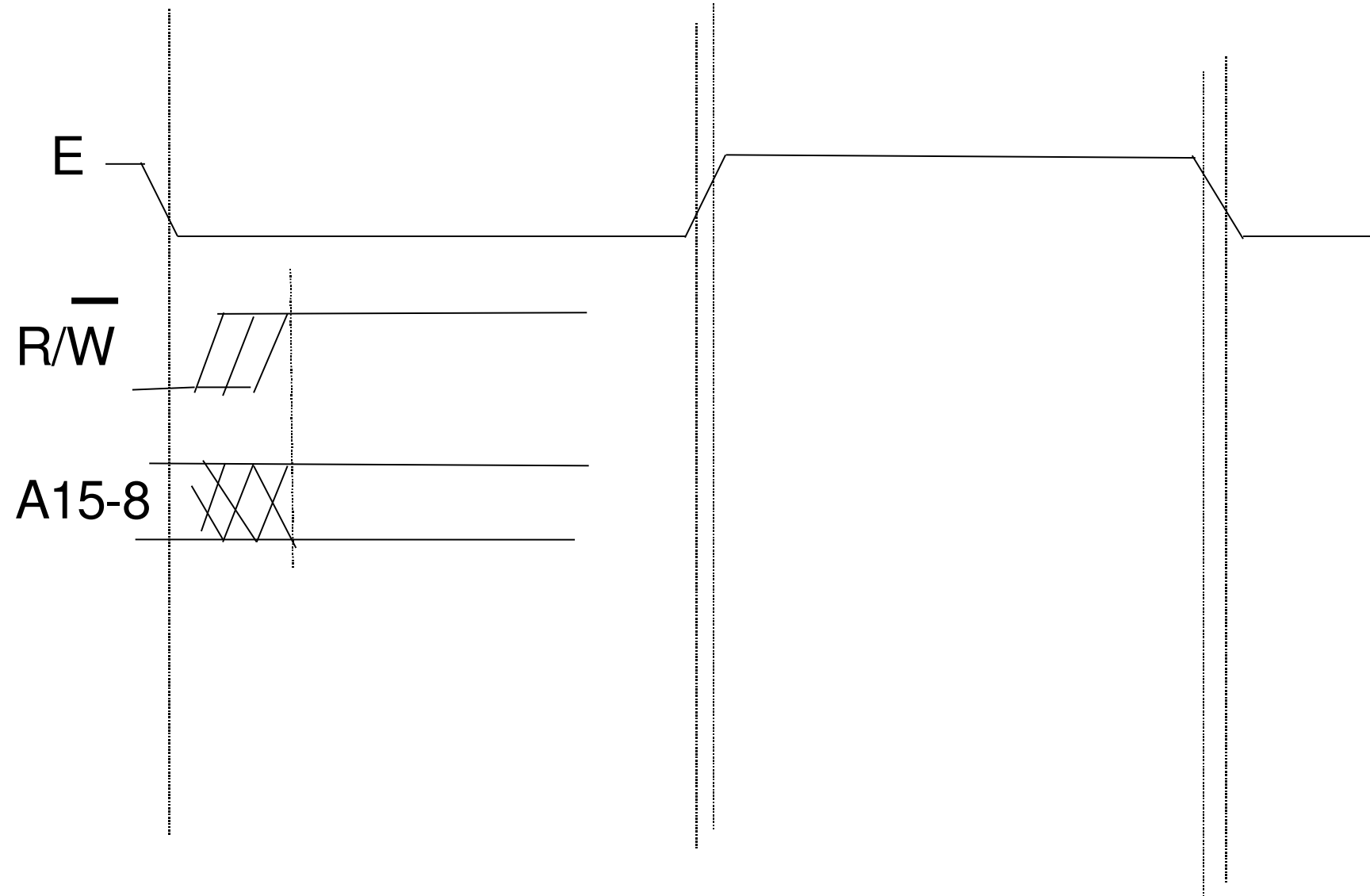
MC68HC11 Read bus cycle



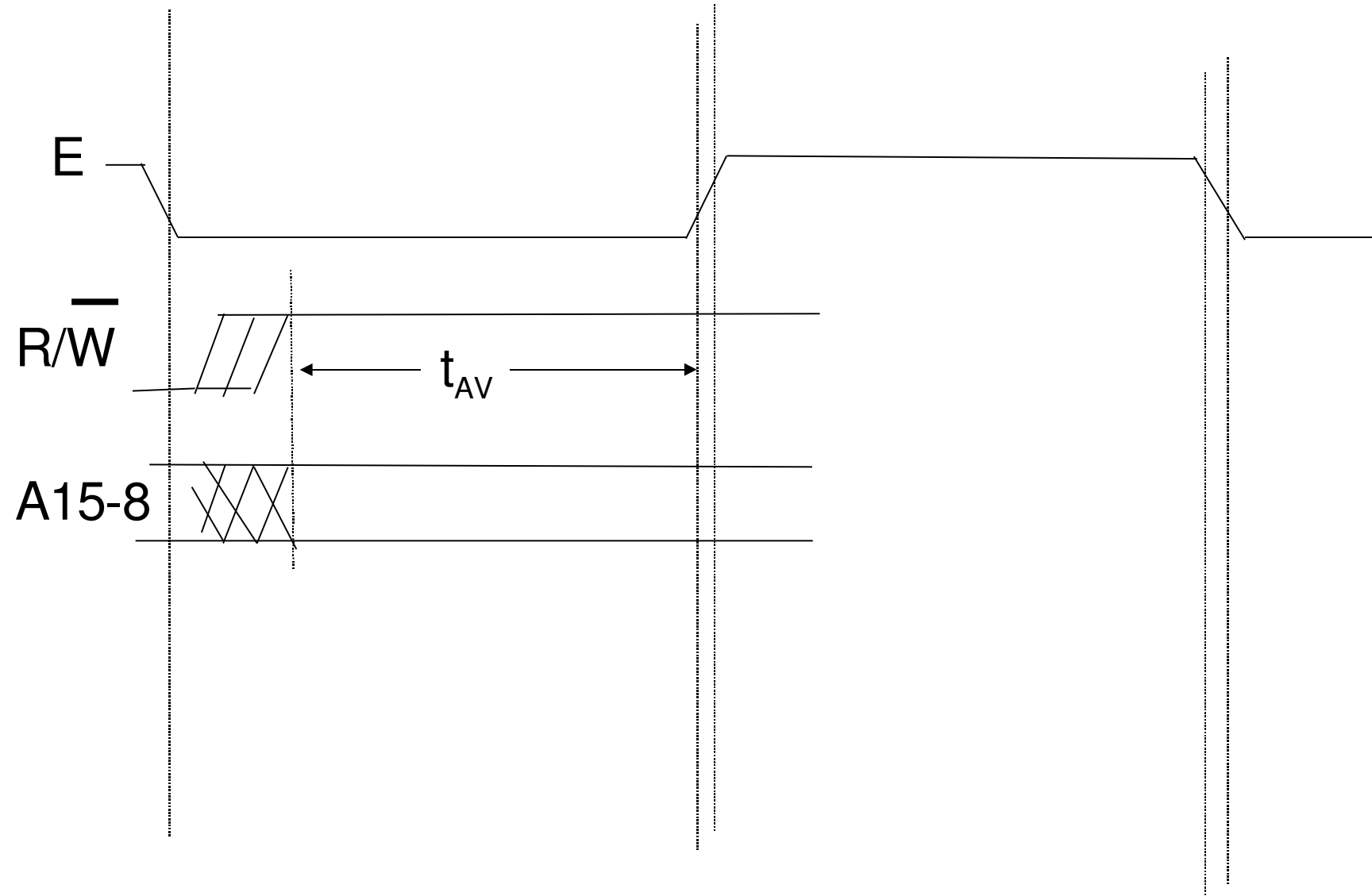
MC68HC11 Read bus cycle



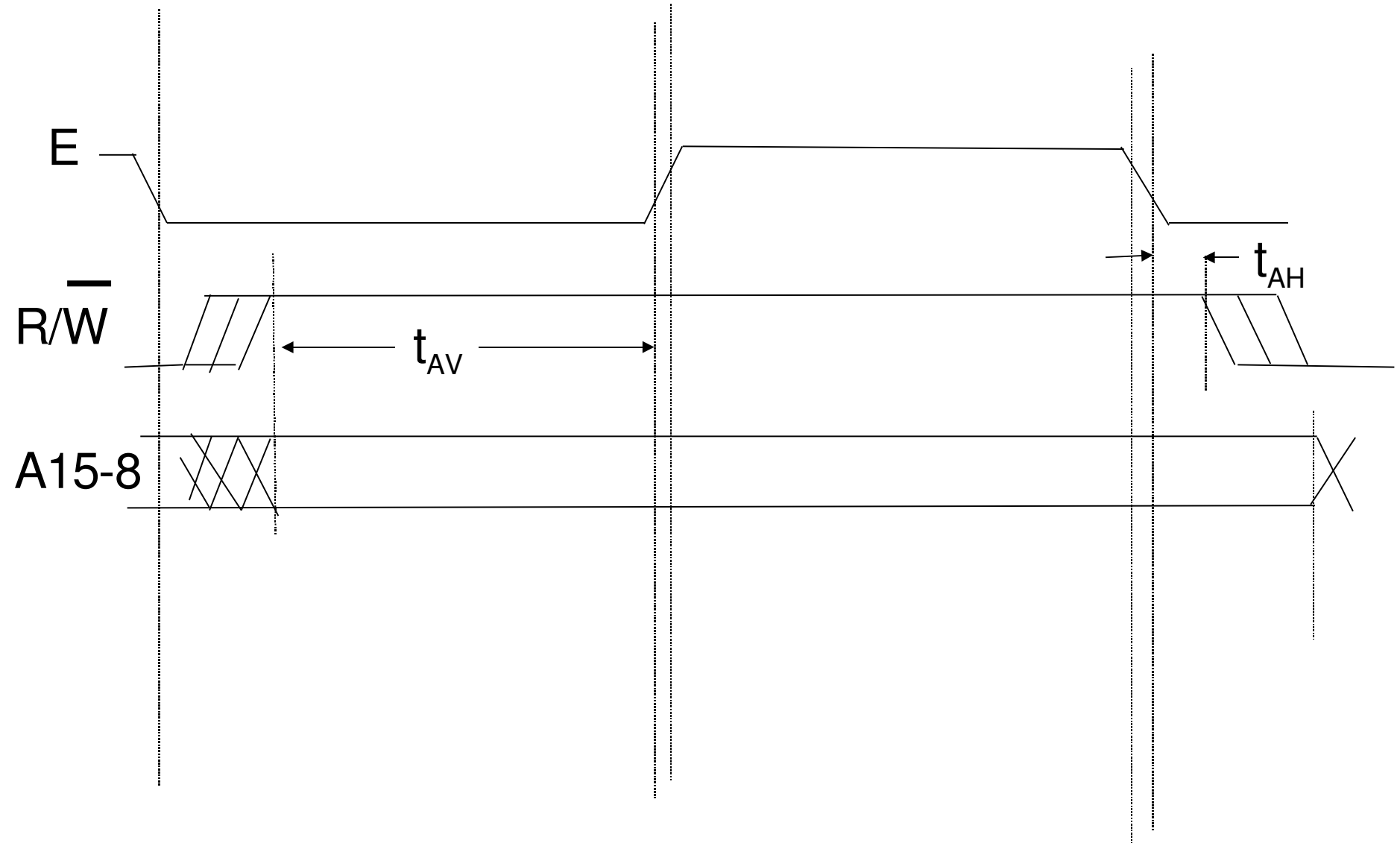
MC68HC11 Read bus cycle



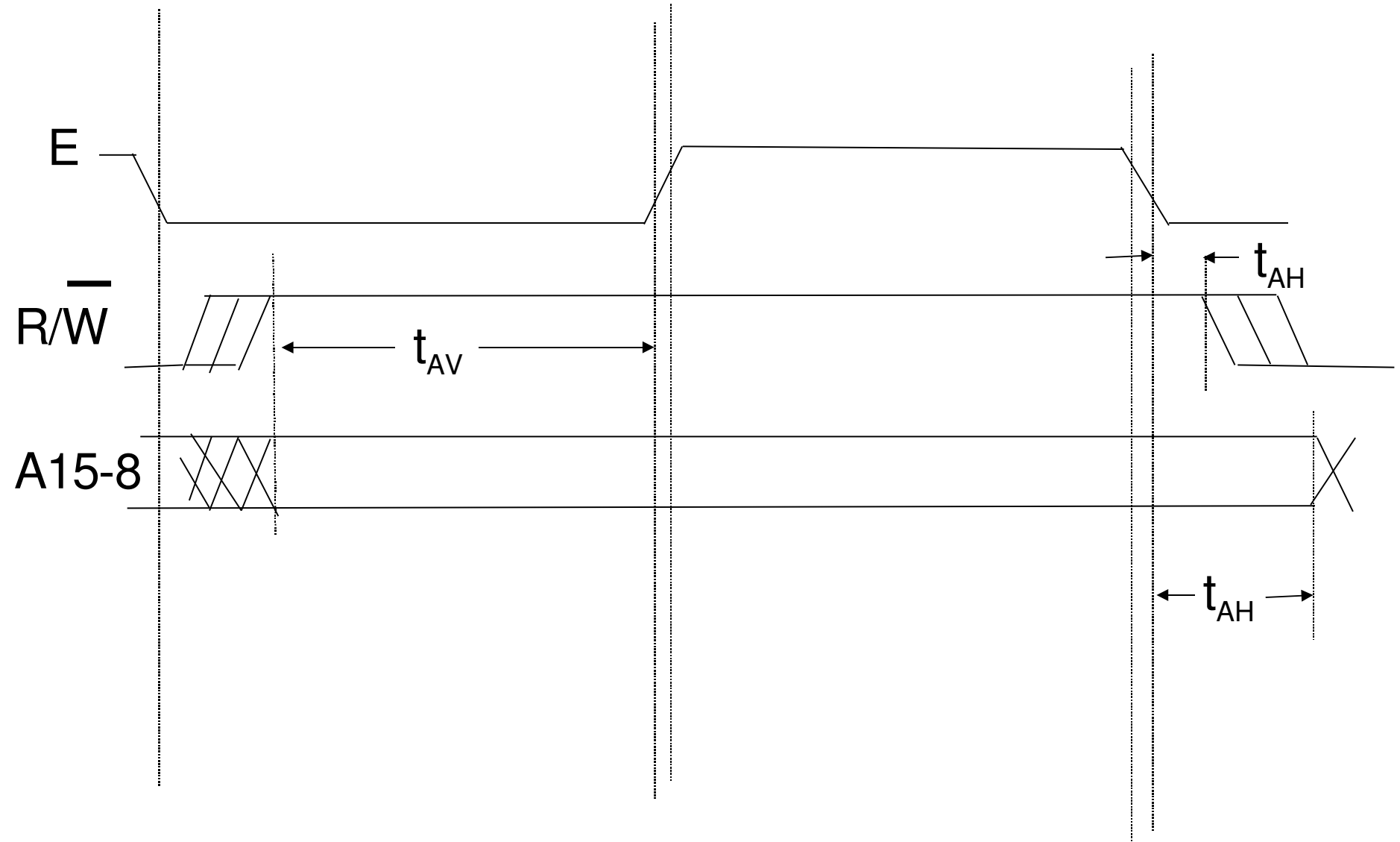
MC68HC11 Read bus cycle



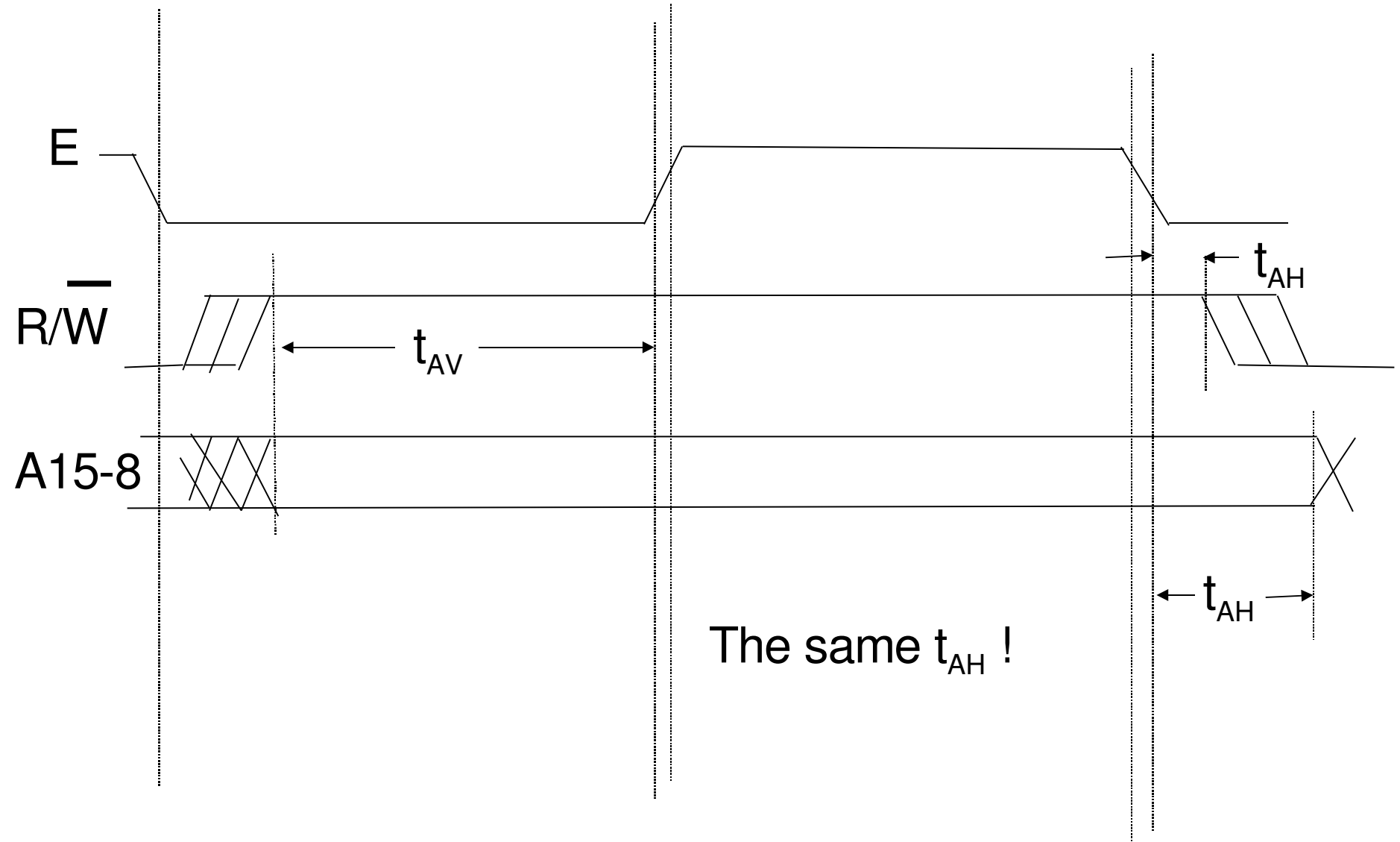
MC68HC11 Read bus cycle



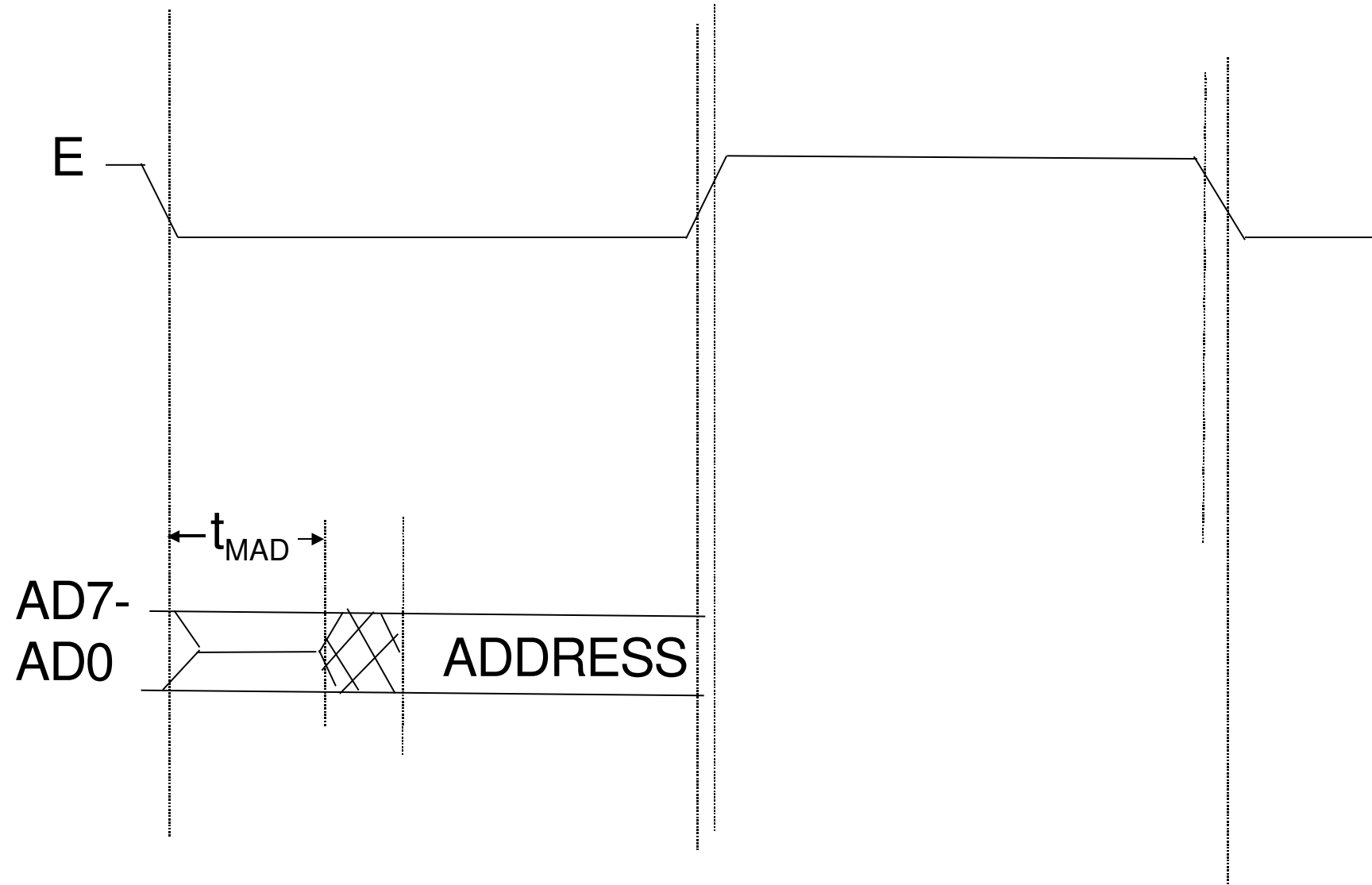
MC68HC11 Read bus cycle



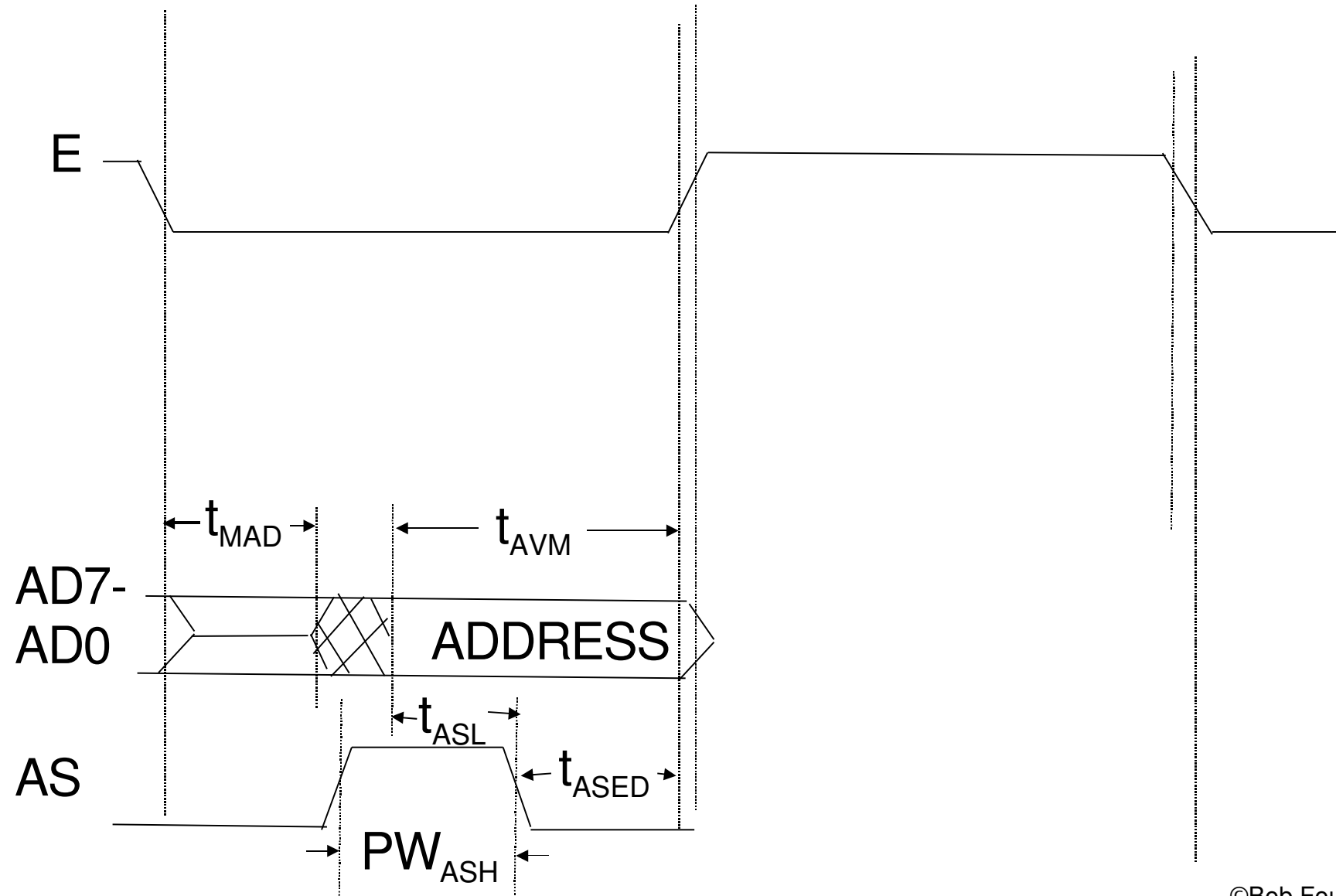
MC68HC11 Read bus cycle



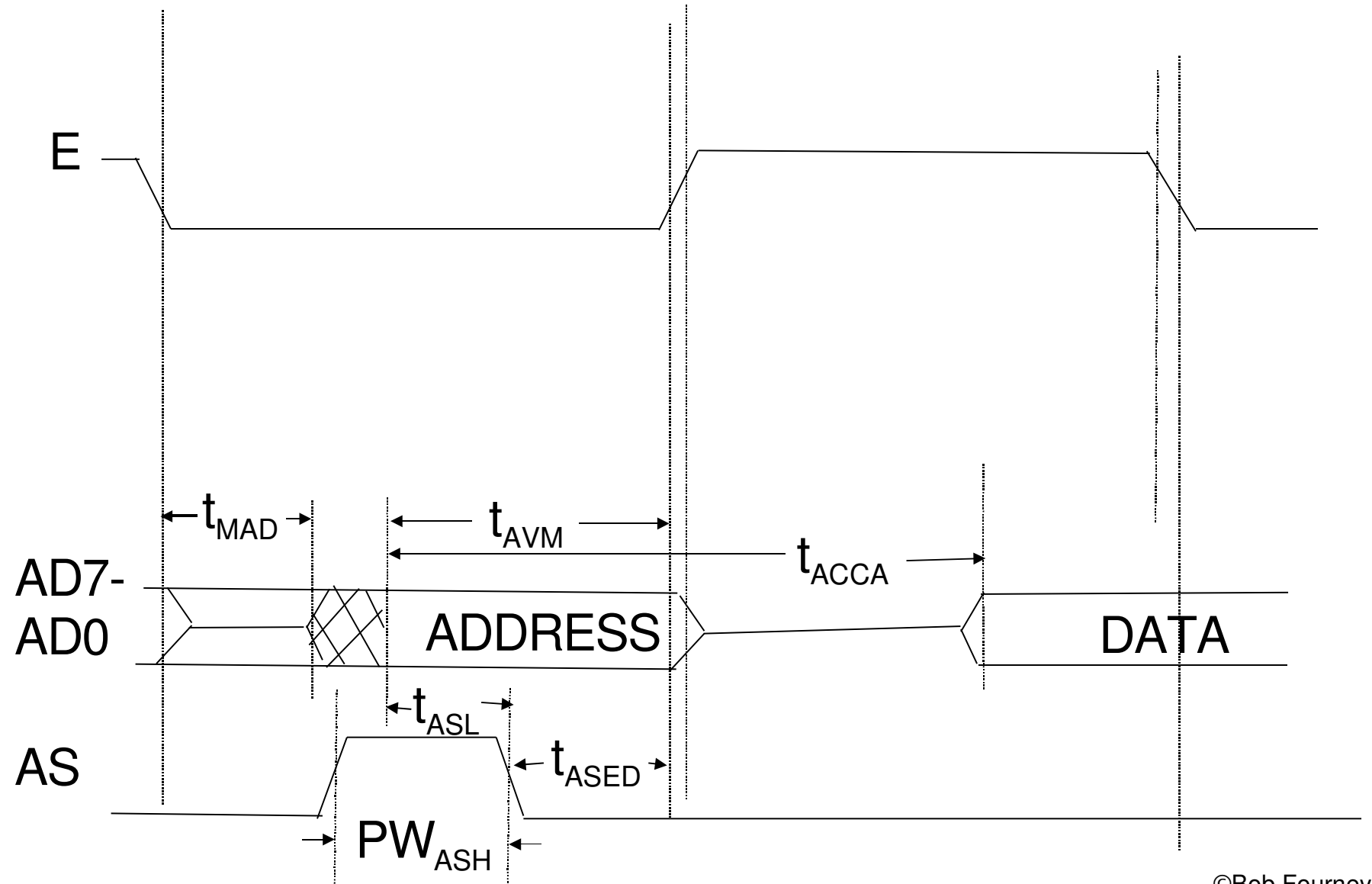
MC68HC11 Read bus cycle



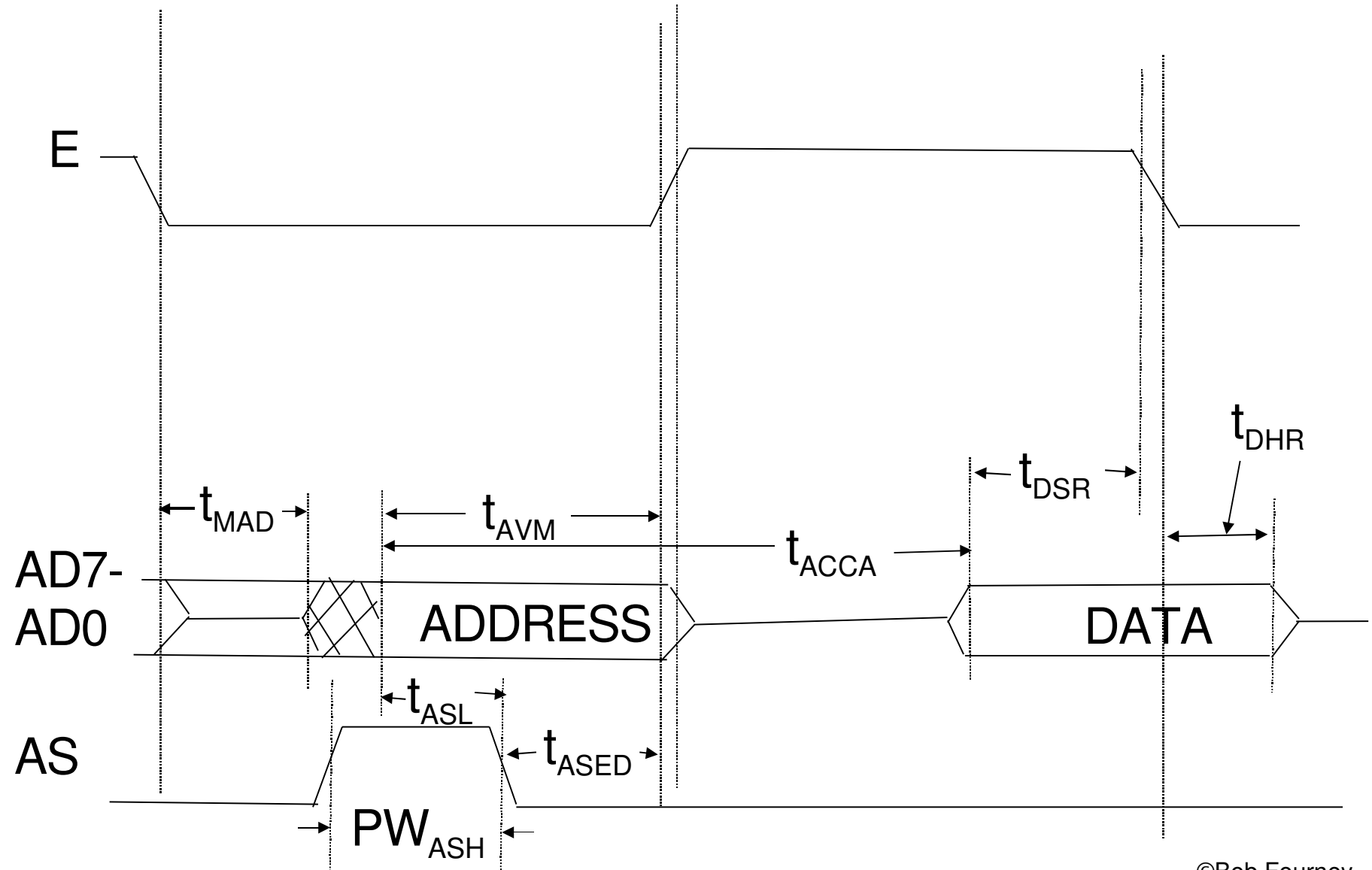
MC68HC11 Read bus cycle



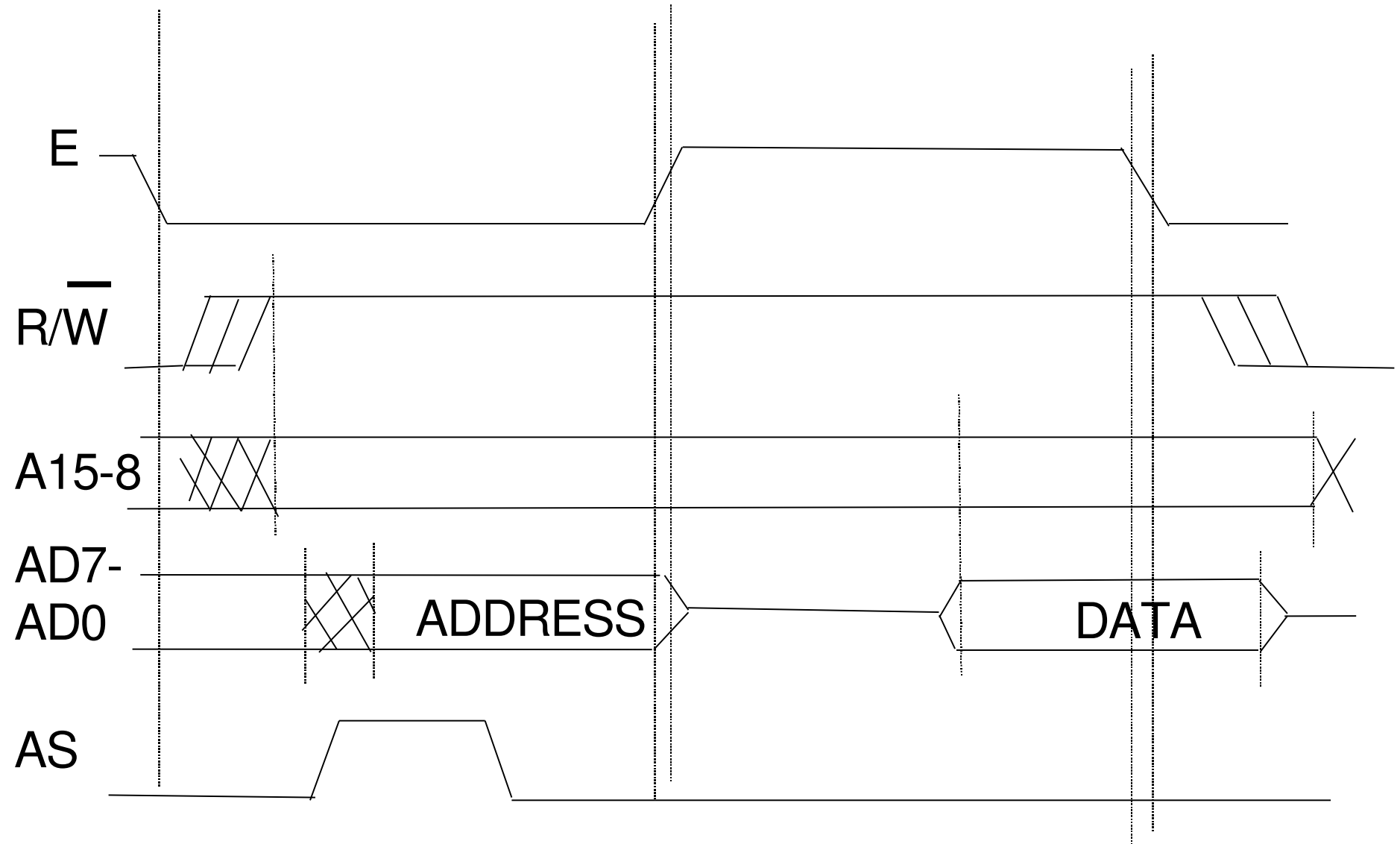
MC68HC11 Read bus cycle



MC68HC11 Read bus cycle



MC68HC11 Read bus cycle



Putting it all Together

Circuit from Figure 5.17 (page 225 in Huang)

Assuming:

74F373 has latch delay of 11.5 nS

74F138 decoder delay is 8 nS

74LS00 and 74LS04 delay is 15 nS